We claim:

1. An integrated circuit component, comprising:

a plurality of connecting contact points;

a plurality of circuit points that are not externally accessible and that provide electrical signals to be measured or analyzed; and

at least one external test connecting contact point to which the signals to be measured or analyzed can be selectively applied such that the signals can be passed on via routes within the integrated circuit component from said plurality of circuit points that are not externally accessible.

2. The integrated circuit according to claim 1, wherein:

said at least one external test connecting contact point is a plurality of external test connecting contact points;

a reference signal is selectively applied and passed on via a route within the integrated circuit component to one of said plurality of external test connecting contact points from one of said plurality of circuit points that are not externally accessible; and

said signals to be measured or analyzed can be selectively applied to be passed on via routes within the integrated circuit component from said plurality of circuit points that are not externally accessible to said plurality of external test connecting contact points other than said one of said plurality of external test connecting contact points.

3. The integrated circuit according to claim 2, wherein said plurality of external test connecting contact points is exactly two external test connecting contact points.

4. The integrated circuit according to claim 1, wherein:

said electrical signals are internal chip signals in the integrated circuit component; and

reference signals and said electrical signals can be selectively passed on to said at least one external test connecting contact point.

5. The integrated circuit according to claim 1, comprising a package and wherein:

said plurality of connecting contact points define a plurality of inaccessible contact points disposed on said package;

said electrical signals at said plurality of circuit points that are not externally accessible are present at said plurality of inaccessible contact points;

said electrical signals and reference signals are selectively passed on to said at least one external test connecting contact point;

and said at least one external test connecting contact point is formed by at least one of said plurality of inaccessible contact points.

6. The integrated circuit according to claim 5, wherein:

said package is a ball grid array package having a lower face;

said plurality of inaccessible contact points are located on said lower face of said package and are thus concealed between said package and a system board on which the package is fitted;

said at least one external test connecting contact point is electrically conductively connected to a corresponding number of metallic test points on the system board.

7. The integrated circuit according to claim 1, wherein a time-controlled multiplexing circuit is provided for selectively passing on the electrical signals to said at least one external test connecting contact point.

8. The integrated circuit according to claim 7, wherein:

said time-controlled multiplexing circuit has inputs and an output and is provided in the integrated circuit component which is surrounded by a ball grid array package;

said plurality of contact points which are not used as external test connecting contact points are electrically conductively connected to said inputs of said multiplexing circuit;

said output of said time-controlled multiplexing circuit is electrically conductively connected to one of said plurality of contact points in the package which forms said at least one external test connecting contact point.

9. The integrated circuit according to claim 7, wherein said multiplexing circuit is programmably controlled to predetermine selective passing on of the electrical signals to said at least one external test connecting contact point.

10. The integrated circuit according to claim 1, wherein said at least one external test connecting contact point can be selectively used in an opposite operating direction for inputting signals to said plurality of circuit points that are not externally accessible.

11. The integrated circuit according to claim 1, wherein said at least one external test connecting contact point is connected to a component tester for analyzing the electrical signals at, at least some of said plurality of circuit points.

12. The integrated circuit according to claim 1, wherein said at least one external test connecting contact point is connected to a system and an application of said system analyzes the electrical signals at, at least some of said plurality of circuit points.

13. The integrated circuit according to claim 1, wherein said at least one external test connecting contact point is used for analyzing a system in which said integrated circuit is used.

14. An integrated circuit component, comprising:

a package;

a plurality of contact points for connection to an external component and disposed on said package;

a test contact point for connection to the external component and disposed on said package; and

a multiplexer having an output connected to said test contact point and having a plurality of inputs, each one of said plurality of inputs connected to a respective one of said plurality of contact points.

15. The integrated circuit according to claim 14, comprising:

a first set of contact points defined by said plurality of contact points;

a second set of contact points for connection to an external component and disposed on said package;

a first test contact point defined by said test contact point;

a second test contact point for connection to the external component and disposed on said package;

a first multiplexer defined by said multiplexer, each one of said plurality of inputs connected to a respective one of said first set of said plurality of contact points; and

a second multiplexer having an output connected to said second test contact point and having a plurality of inputs, each one of said plurality of inputs of said second multiplexer connected to a respective one of said second set of contact points.

16. The integrated circuit according to claim 14, wherein said package is a ball grid array package.